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OP-S10GDT-80
Tunable SFP+ 10G DWDM Optical Transceiver 80km DDM

1. Key Features

- ITU-T C-band 50 GHz spacing tunable DWDM SFP+ transceiver
- Data rate 9.95-11.3 Gbps
- Supports 80 km link distances
- Negative chirp transmitter with ILMZ (integrated laser Mach Zehnder) TOSA
- APD receiver with limiting amplifier
- Positive power supply lines: 3.3 V
- Operating case temperature range: up to industrial temperature
- Compact size (56.5 mm L x 13.9 mm W x 11.85 mm H)

2. Compliance

- SFF-8431 – Enhanced 8.5 and 10 Gigabit Small Form Factor Pluggable Module
- SFF-8432 - Improved Pluggable Form factor
- SFF-8690 - Tunable SFP+ Memory Map for ITU Frequencies
- SFF-8472 - Diagnostic Monitoring Interface for Optical Xcvrs
- INF-8074i - SFP (Small Form Factor) Transceiver
- IEEE802.3ae CL 52 - IEEE 802.3 Standard (10Gigabit Ethernet Clause)
- MIL-STD-883, Method 3015.4
- IEC61000-4-2:Edition1 (Air Discharge)
- Class 1 Laser Safety

3. Product Description

OPTINET Tunable SFP+ module is a high performance tunable pluggable transceiver for use in the C-band window covering 1528 nm to 1566 nm. The module supports data rates from 9.95 Gbps to 11.3 Gbps and is provided in an SFP+, MSA-compliant package.

The optical transmitter utilizes the Lumentum tunable ILMZ chip to provide a high performance, low cost 10 Gbps transceiver. Channel tuning is supported on the ITU-T 50 GHz grid across full C band with ±2.5 GHz stability. Wavelength and frequency tuning modes are supported in accordance with SFF-8690.The receive path comprises an APD receiver with limiting amplifier.

4. Functional Description

(1) SFI Data Interface

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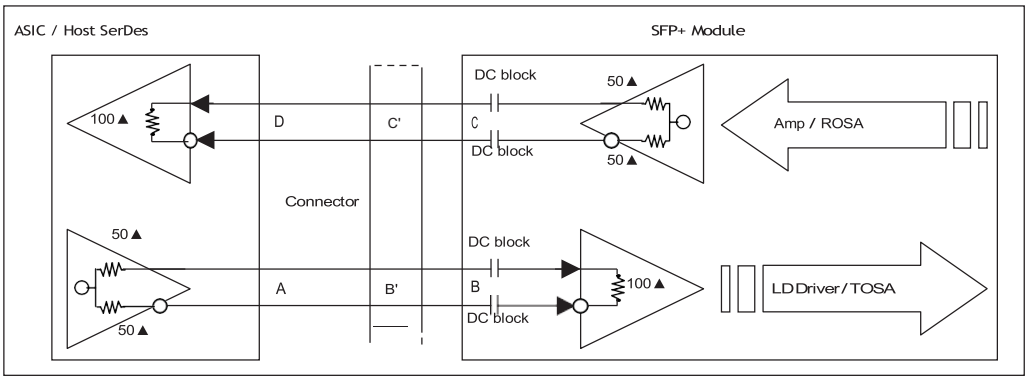


Figure 1 Interface to host

Table 1: SFP+ Module Transmitter Electrical Characteristics at B"

Parameter @ B''	Symbol	Minimum	Maximum	Units
Eye mask	X1		0.12	UI
Eye mask	X2		0.33	UI
Eye mask	Y1	95		mV
Eye mask	Y2		350	mV

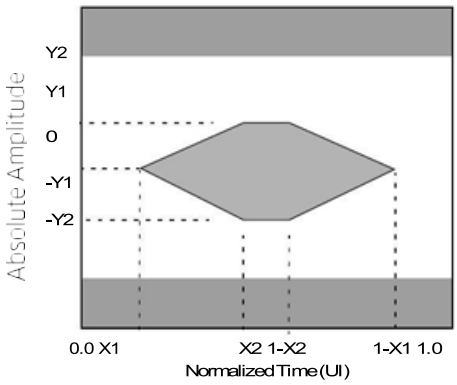
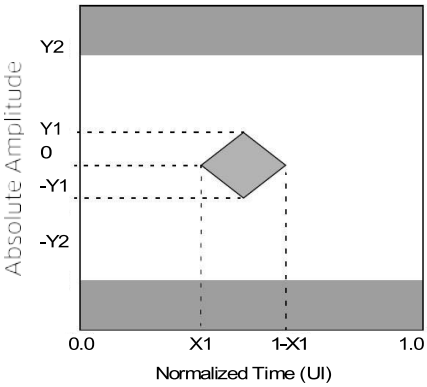


Figure 2 Eye mask at B''

Table 2: SFP+ Module Receiver Electrical Characteristics at C'

Parameter @ C'	Symbol	Minimum	Maximum	Units
Eye Mask	X1		0.35	UI
Eye Mask	Y1	150		mV
Eye Mask	Y2	-	425	mV



4. Low Speed Control Pins

- TX_Fault
- TX_Disable
- Mod_ABS
- RX_LOS

Table 3: Low Speed Control Pin Logic Levels

Parameter	Symbol	Minimum	Maximum	Unit	Conditions
Host V_{CC} Range	Host_V_{CC}	3.14	3.47	V	with ± 5% variation
TX_Fault, RX_LOS	V_{OL}	0.0	0.40	V	Note 1
	V_{OH}	Host_V_{CC} – 0.5	Host_V_{CC} + 0.3	V	Note 1
TX_Disable	V_{IL}	-0.3	0.8	V	Pulled up with 10k ohms to V_{CC}T in the module.
	V_{IH}	2.0	V_{CC}T + 0.3	V	

Note:
1. Rpullup (Rp) is the pull up resistor. Active bus termination may be used by the host in place of a pullup resistor. Pull ups can be connected to multiple power supplies, however the host board design shall ensure that no module pin has voltage exceeding module. Measured at the Host side of the connector.
TX_Fault is a module output pin that when High, indicates that the module transmitter has detected a fault condition related to laser operation or safety. The TX_Fault output pin is an open drain/collector and must be pulled up to the Host_Vcc with 4.7k-10kΩ on the host board
TX_Disable is a module input pin. When TX_Disable is asserted High or left open, the SFP+ module transmitter output must be turned off. The TX_Disable pin is pulled up to VccT with 10kΩ in the SFP+ module. The TX_Disable pin works for TX_fault_Reset as well.Mod_ABS is pulled up to Host_Vcc with 4.7k-10kΩ on the host board and connected to VeeT or VeeR in the SFP+ module. Mod_ABS is then asserted “High” when the SFP+ module is physically absent from a host slot. In the SFP MSA (INF8074i) this pin had the same function but is called MOD_DEF0.
RX_LOS when high indicates an optical signal level below that specified in the relevant standard. The RX_LOS pin is an open drain/ collector output and must be pulled up to host Vcc with a 4.7k-10kΩ on the host board. RX_LOS assert min and de-assert max are defined in the relevant standard.

5. 2-Wire Interface I2C: SDA & SCL

SCL is the 2-wire interface clock and SDA is the 2-wire interface data line. SCL and SDA are pulled up with a voltage in the range of 3.14 V to 3.47 V on the host. SFP+ low speed interface is based on 2-wire interface. SFP+ 2-wire interface is based on low voltage TTL (LVTTL) operating with a supply of 3.3 V ±5% and are given in Table 4. This specification ensures compatibility between host masters and SFP+ SCL/SDA lines and compatibility with I2C. All voltages are referenced to VeeT.

Note:
After an interruption in protocol, power loss or system reset, the 2-wire part can be reset by following these steps:
- Clock up to 9 cycles.
- Look for SDA high in each cycle while SCL is high.
- Create a start condition.

Table 4:2-Wire Interface Physical Interface

Parameter	Symbol	Min.	Max.	Unit	Conditions
Host V_{CC} range	Host_V_{CC}	3.14	3.47	V	

SCL and SDA	V_{OL}	0.0	0.40	V	Rpullup[1] pulled to Host_V_{CC}. I_{OL}(max) = 3 mA
	V_{OH}	Host_V_{CC} – 0.5	Host_V_{CC} + 0.3	V	Rpullup[1] pulled to Host_V_{CC}
SCL and SDA	V_{IL}	-0.3	V_{CC}T *0.3T	V	
	V_{IH}	V_{CC}T * 0.7	V_{CC}T + 0.5	V	
Input current on SCL and SDA pins	I_L	-10	10	μA	
Capacitance on SCL and SDA pins	C_i 2		14	pF	
Total bus capacitance for SCL and SDA	C_b 3		100	pF	At 400 kHz, R_p (max) = 3.0 kΩ At 100 kHz, R_p (max) = 8.0 kΩ
			290	pF	At 400 kHz, R_p (max) = 1.1 kΩ At 100 kHz, R_p (max) = 2.75 kΩ

Note:
Rpullup (Rp) is the pull up resistor. Active bus termination may be used by the host in place of a pullup resistor. Pull ups can be connected to multiple power supplies, however the host board design shall ensure that no module pin has voltage exceeding module. M easured at the Host side of the connector. VccT/R + 0.5 V nor requires the module to sink more than 3.0 mA current.

- Ci is the capacitance looking into the module SCL and SDA pins
- Cb is the total bus cap acitance on the SCL or SDA bus

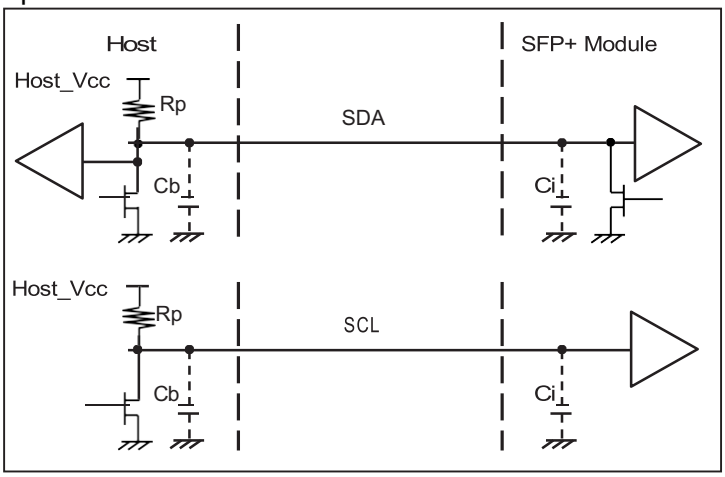


Figure 4 2-Wire interface physical interface

Table 5: SFP+ 2-Wire Interface Timing Requirements

Parameter	Symbol	Minimum	Maximum	Unit	Conditions
Clock frequency	f_{SCL}	100	400	kHz	
Clock pulse width low	t_{LOW}	1.3		μs	
Clock pulse width high	t_{HIGH}	0.6		μs	
Time bus free before new transaction can start	t_{BUF}	20		μs	Between STOP and START
START hold time	$t_{HD,STA}$	0.6		μs	

START set-up time	$t_{SU,STA}$	0.6		μs	
Data in hold time	$t_{HD,DAT}$	0		μs	
Data in set-up time	$t_{SU,DAT}$	0.1		μs	
Input rise time (100 kHz)	$t_{R,100}$		1000	ns	Note 1
Input rise time (400 kHz)	$t_{R,400}$		300	ns	Note 1
Input fall time (100 kHz)	$t_{F,100}$		300	ns	Note 1
Input fall time (400 kHz)	$t_{F,400}$		300	ns	Note 1
STOP set-ip time	$t_{SU,STO}$	0.6		μs	
Serial interface clock holdoff "clock stretching"	T_clock_hold		500	μs	Maximum time the SFP+ may hold the SCL line low before continuing R or W operation
Complete single or sequential write	t_{WR}		40	ms	Complete (up to) 8 Byte write
Endurance (write cycles)		10 k		Cycles	@ Max operating temperature

Note:

1. From (VIL, MAX – 0.15) to (VIH, MIN + 0.15)

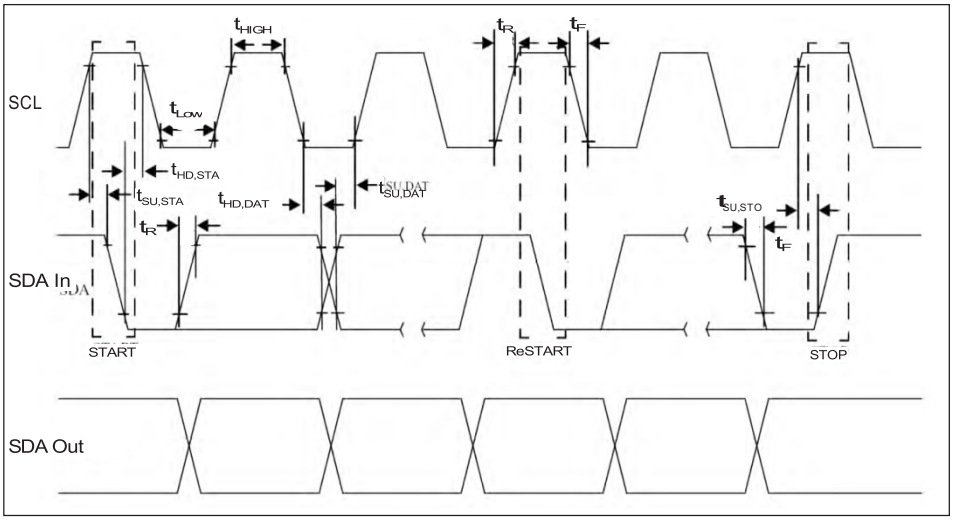


Figure 5 SFP+ timing diagram

6. SFP+ Module Timing

In the below figures are shown the required timing for TX_Fault and TX_Disable in various conditions.

Table 6:SFP+ Timing Requirements

Parameter	Symbol	Minimum	Maximum	Unit	Conditions
TX_disable assert time	t_off		100	μs	Rising edge of TX_Disable to fall of output signal below 10% of nominal.
TX_disable negate time	T_on		2	ms	Falling edge of TX_Disable to rise of output signal above 90% of nominal. This only applies in normal operation, not during start up or fault recovery.

Time to initialize 2-wire interface	t_2w_ start_up		300	ms	From power on or hot plug after the supply meeting Table 9.
Time to initialize cooled module and time to power up a cooled module to Power Level II	t_start_ up_c ooled		90	sec	From power supplies meeting Table 9 or hot plug, or Tx disable negated during power up or Tx_Fault recovery, until cooled power level II part during fault recovery is fully operational. Also, from stop bit low-to-high SDA transition enabling Power Level II until cooled module is fully operational
Tx_fault assert for cooled module	Tx_fault_ on_cooled		1	ms	From occurence of fault to assertion of TX_Fault
Tx_fault_reset	t_reset	10		μs	Time TX_disable must be held high to reset TX_Fault.
RX_LOS assert delay	t_los_on		100	μs	From occurrence of loss of signal to assertion of RX_LOS.
RX_LOS negate delay	t_los_off		100	μs	From occurrence of presence of signal to negation of RX_LOS.

7. Maximum Current Ramp on Power supply

In the below figure and table are shown the required inrush current characteristics for the module power pins.

Table 7: Inrush Current

Parameter	Symbol	Minimum	Maximum	Unit	Remarks
Icc instantaneous peak current			600	mA	Note 1, 2
Icc sustained peak current			500	mA	Note 1, 2

Note:
The maximum currents are the allowed currents for each power supply VccT or VccR, therefore the total module peak currents can be twice this value. The instantaneous peak current is allowed to exceed the specified maximum current capacity of the connector contact for a short period.
Not to exceed the sustained peak limit for more than 50 μs; may exceed this limit for shorter durations

8. Performance Specifications

(1) Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the transceiver.

Table 8: Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Unit	Remarks
Supply voltage	$V_{CC}T$	0	+3.6	V	+3.3 V
Supply voltage	$V_{CC}R$	0	+3.6	V	+3.3 V
Optical receiver input	P_{IMAX}		+5	dBm	Average
Storage temperature	T_{STR}	-40	+85	°C	
ESD SFI pins	ESD1		1	kV	HBM
ESD except for SFI pins	ESD2		2	kV	HBM

(2) Operating Environment

Electrical and optical characteristics below are defined under this operating environment, unless otherwise specified.

Table 9: Operating Environment

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Remarks
Supply voltage	$V_{CC}T$	3.135	3.300	3.465	V	+3.3 V
Supply voltage	$V_{CC}R$	3.135	3.300	3.465	V	+3.3 V
Operating case temperature	T_C	0		+70	°C	C-temp
		-5		+85		E-temp
		-40		+85		I-temp

9. Optical Interface Characteristics

Table 10: Optical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Remarks
Transmitter						
Data rate		9.95		11.3	Gbps	NRZ
Frequency range		191.35		196.10	THz	50 GHz grid, 96 channels
Frequency accuracy		-2.5		+2.5	GHz	EOL
Optical transmit power	Po	-1.0		+3.0	dBm	EOL
Shuttered output power				-35	dBm	
Optical power stability	ΔPo	-1.0		+1.0	dB	All channels, SOL
Side mode suppression	SMSR	35			dB	±2.5 nm, modulated
Spectral width	Δλ		0.3	0.5	nm	-20 dB, modulated
Extinction ratio	ER	9.0			dB	Filtered, 10.709 Gbps
Eye diagram compliance		GR-253, ITU-T G.691				
Mask margin		10			%	
Tuning speed				10	s	Warmed-up, from any CH to any other CH
Receiver						
Data rate		9.95		11.3	Gbps	NRZ
Input operating wavelength		1525		1575	nm	
Minimum receiver sensitivity (back to back)	Prmin			-24	dBm	10.709 Gbps, 1E-12, OSNR>35 dB
Minimum receiver Sensitivity (-300~+1400 ps/nm)	Prmin	0		-21	dBm	
Maximum input power (overload)	Pro	-7			dBm	
Receiver Reflectance	RL			-27	dB	
LOS assert				-27	dBm	Note 1
LOS de-assert				-25	dBm	Note 1

LOS hysteresis		0.5		4.0	dB	Note 1
LOS assert time				100	us	
LOS de-assert time				100	us	

Note 1:

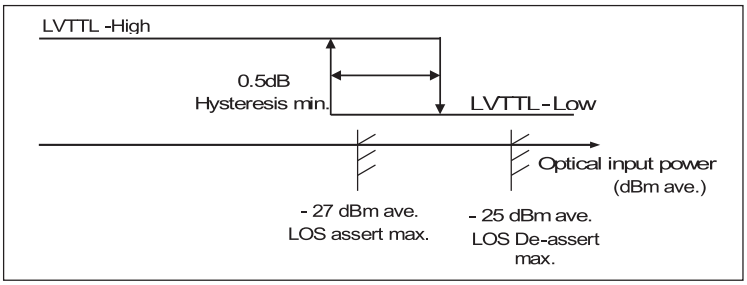


Figure 6 Rx LOS assert and de-assert

10. Pin out Definition

Table 11: Pin Description

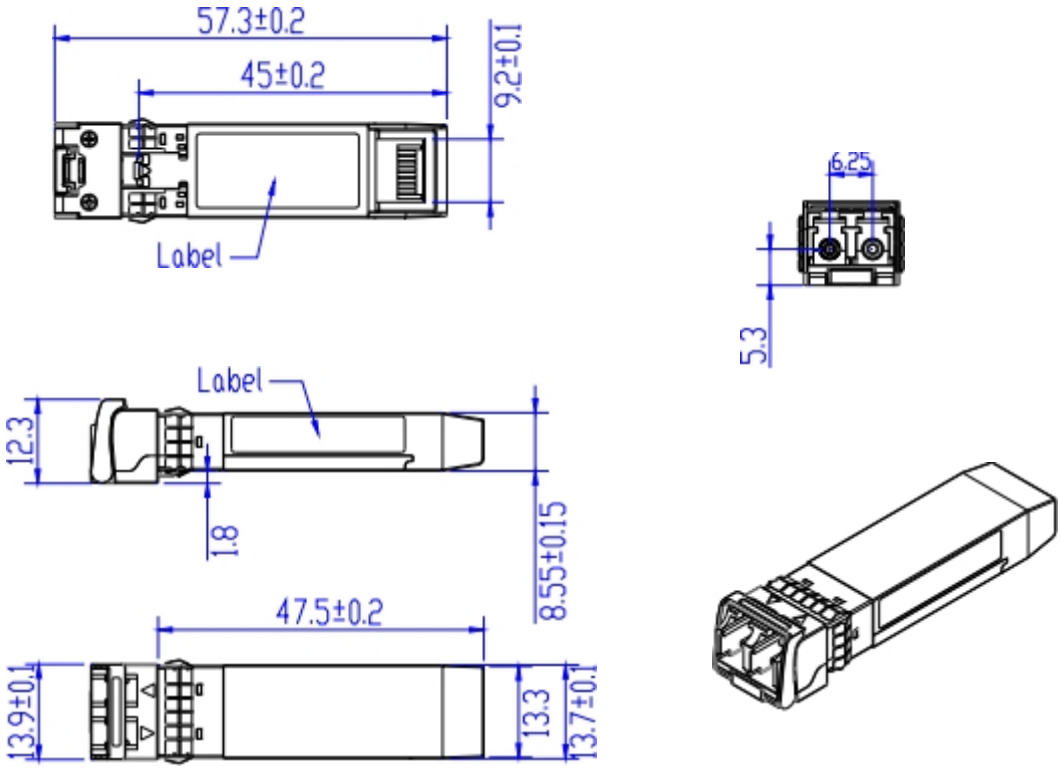
Pin	Logic	Symbol	Power Sequence Order	Name/Description	Notes
1		VeeT	1st	Module Transmitter Ground	1
2	LVTTL-O	TX_Fault	3rd	Module Transmitter Fault	2
3	LVTTL-I	TX_Disable	3rd	Transmitter Disable; Turn off laser output	3
4	LVTTL-I/O	SDA	3rd	2-Wire Serial Interface Data Line	4
5	LVTTL-I/O	SCL	3rd	2-Wire Serial Interface Clock	4
6		Mod_Abs	3rd	Module Absent, connected to VeeT or VeeR in the module	5
7	LVTTL-I	RS0	3rd	NA. 30kohm pull down inside the module	
8	LVTTL-O	RX_LOS	3rd	Receiver Loss of Signal Indicator	2
9	LVTTL-I	RS1	3rd	NA. 30kohm pull down inside the module	
10		VeeR	1st	Module Receiver Ground	1
11		VeeR	1st	Module Receiver Ground	1
12	CML-O	RD-	3rd	Receiver Inverted Data Output(SFI)	
13	CML-O	RD+	3rd	Receiver Non-Inverted Data Output(SFI)	
14		VeeR	1st	Module Receiver Ground	1
15		VccR	2nd	Module Receiver 3.3V Supply	6
16		VccT	2nd	Module Transmitter 3.3V Supply	6
17		VeeT	1st	Module Transmitter Ground	1

18	CML-I	TD+	3rd	Transmitter Non-Inverted Data Output(SFI)	
19	CML-I	TD-	3rd	Transmitter Inverted Data Output(SFI)	
20		VeeT	1st	Module Transmitter Ground	1

Note:

The module signal ground pins, VeeR and VeeT, are isolated from the module case.
This pin is an open drain output pin and shall be pulled up with 4.7 k-10 kohms to Host_Vcc (Table3) on the host board. Pull ups can be connected to multiple power supplies, however the host board design shall ensure that no module pin has voltage exceeding module VccT/R + 0.5 V.
This pin is an input pin with 10kohms pull up to VccT in the module.
See table 4 and 2-Wire Electrical Specifications .
This pin shall be pulled up with 4.7 k-10 kohms to Host_Vcc on the host board.
VccT and VccR are tied together inside the module.

11. Mechanical Dimension



12. Ordering Information

Part No	Data Rate	Wavelength	Reach	Temp	DDM
OP-S10GDT-80	10Gbps	1568~1529	80KM	0~70°C	Yes